SLAC-PUB-9806
May, 2003

HIGH RESOLUTION ANALOG / DIGITAL POWER SUPPLY CONTROLLER*

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Abstract

Corrector magnets for the SPEAR-3 synchrotron radiation source require precision, high-speed control for use with beam-based orbit feedback. A new Controller Analog/Digital Interface card (CANDI) has been developed for these purposes. The CANDI has a 24-bit DAC for current control and three 24-bit Δ-Σ ADCs to monitor current and voltages. The ADCs can be read and the DAC updated at the 4 kHz rate needed for feedback control. A precision 16-bit DAC provides on-board calibration. Programmable multiplexers control internal signal routing for calibration, testing, and measurement. Feedback can be closed internally on current setpoint, externally on supply current, or beam position. Prototype and production tests are reported in this paper. Noise is better than 17 effective bits in a 10 mHz to 2 kHz bandwidth. Linearity and temperature stability are excellent.

OVERVIEW

Each magnet for orbit correction at SPEAR 3 will have a bipolar ±30 A supply, the MCOR [1]. One MCOR supply with CANDI daughter board occupies two slots in a 17-slot crate. One crate can support 8 MCORs. The CANDI board controls and monitors the supply's current and voltage, exchanges data with the interface board and the standard VME processor via the crate backplane. The processor plugs into the interface board, which adapts the VME processor to the MCOR crate.

CANDI BOARD DESCRIPTION

The 170 CANDI boards were fabricated and assembled. The CANDI board size is 6.5" x 3.95", about 0.062" thick. A shielding box covers the analog signal processing area. Figure 1 shows a module block diagram.

At the front of the CANDI card there is 4-digit LED display, showing the supply's current value and interlock status; the RS232 input, and the connector for re-programming the FPGA (Field Programmable Gate Array) boot PROM.

Two connectors go to the supply. One transmits the MCOR interlock signals. The other provides the current setpoint to the supply, it carries the output current to the magnet and monitor lines for the 65 Volt bulk supply, the output voltages, and the output current. The short buses connect the supply's signals with the output connector, plugging to the crate backplane. The supply's output signal is split in such a way that half load current goes through the supply's connector and half through the CANDI board connector.

The FPGA executes the processor's commands, reads status, writes and reads three ADCs and two DACs.

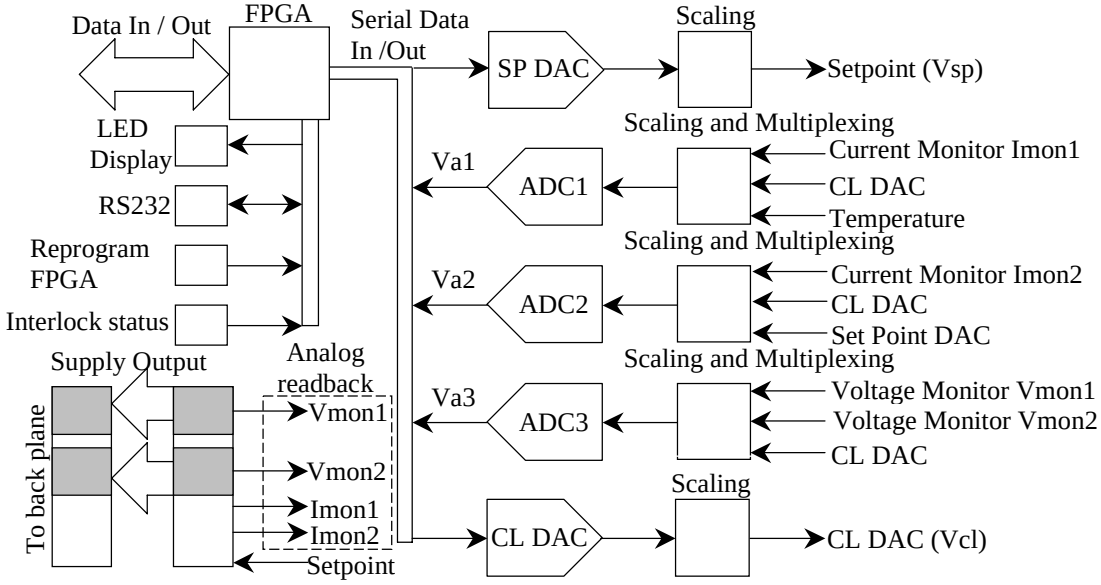

Figure 1. The CANDI block diagram.

*Work supported in part by Department of Energy Contract DE-AC03-76SF00515 and Office of Basic Energy Sciences, Division of Chemical Sciences.

The 24-bit resolution Set Point DAC (SP DAC), a Burr-Brown PCM1704, sets the MCOR control voltage from 0V to ±10 V to control the MCOR output current from 0 to ±30 A. Three 24-bit resolution Δ-Σ ADCs, a Burr-Brown ADS1251, digitize analog signals - the Imon1, Imon2, Vmon1 and Vmon2 [2]. A precision 16-bit DAC, a Maxim MAX542 [3] is dedicated to calibration of the ADCs (CL DAC).

The highest ADC output rate frequency is 20.8 MHz at an input clock frequency 8 MHz, the internal digital filter has notches at the output rate frequency and harmonics. The ADC has a fixed over-sampling ratio of 64.

Dual 4-channel multiplexers (MUX) are placed in the front of the signal processing chain. This provides for module calibration, and configuration of local, remote, or global feedback.

REQUIREMENTS

- Required data update frequency 4 kHz.

The analog setpoint and the readback requirements are shown below (Table 1 and Table 2).

Table 1. The current setpoint requirements.

Analog Setpoint	**Requirements**
Full scale voltage range	± 10 V
Bandwidth	DC - 2 kHz
Accuracy	± 10 mV
Stability (24 hours, ± 3.5 °C)	± 500 µV
Signal to Noise Ratio, integrated over 10 mHz - 2 kHz	105 dB or 17.2 ENOB

- The temperature coefficient limit is: 14.3 ppm/°C (± 500 µV / ± 3.5 °C, out of 10 V full scale).

Table 2. The current monitor readback requirements.

Analog Readback, Imon	**Requirements**
Full scale voltage range	± 10 V
Bandwidth	DC - 2 kHz
Accuracy	± 1 mV
Signal to Noise Ratio integrated over 1 Hz - 200 Hz	101 dB or 16.6 ENOB
Analog Readback, Vmon	
Full scale voltage range	70 V
Accuracy	± 10 mV
Signal to Noise Ratio, integrated over 1 Hz - 1 kHz	86 dB or 14 ENOB

The ENOB is the Effective Number of Bits, Signal to Noise Ratio = 6.02 dB * ENOB + 1.76 dB.

RESULTS

Accuracy

The following scheme was used to measure accuracy (Fig. 2). The SP DAC and the CL DAC are swept across a -10 V to +10V range in 2 V steps. The SP DAC output signal (Vsp) goes to the external Data Acquisition Unit (Vref) and to the ADC2 (Va21) via the multiplexer. After reading them, the multiplexer connects the ADC2 input to the CL DAC output (Vcl); the ADC1 and ADC3 are already connected to the CL DAC. One cycle of the measurements ends when ADC1 (Va1), ADC2 (Va22) and ADC3 (Va3) are read. A linear fit yields the relative gain and zero offset. Calibration results are saved for operational use.

Calibrated data and source signal differences are within the ± 300 µV peak-to-peak; the rms is 123 µV, better than required.

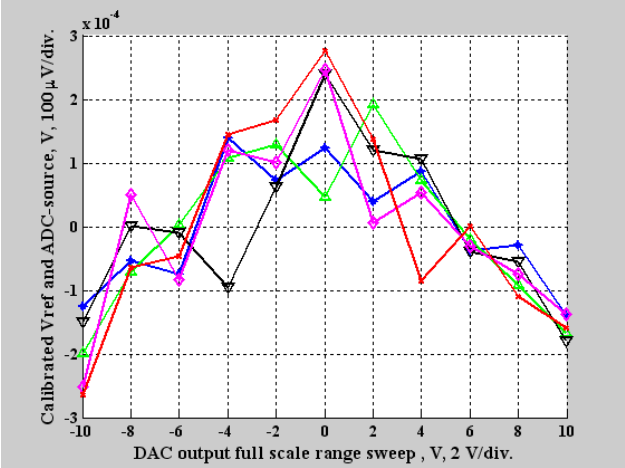

Figure 2. The setpoint and the readback accuracy.

The noise performance

The ENOB measurements were performed at 4 kHz data update frequency and 20 kHz ADC readback rate. The SP and CL DAC outputs were set to + full scale. In addition to the ADC 64 oversamplings, the FPGA averages 16 ADC samples. This is equivalent to increasing the ADC oversampling ratio a factor of 4. The set point and the read back ENOB spread is shown on the Table 3 below.

Table 3. The setpoint and readback ENOB.

Source signal to ADC #	**ENOB**	
	min	**max**
Setpoint: SP DAC to ADC2	17.3	17.7
Readback: CL DAC to ADC1 & 2	17.5	18.0
Readback: CL DAC to ADC3	17.0	17.9

The production module has no additional averages, the ADC output rate is 4 kHz, the readback ENOB is reduced another 1.25 bits.

Stability

Stability is tested by observing the setpoint output voltage for extended periods at fixed DAC setting near full scale. For example Figure 3 shows the setpoint output varying 1.1 mV over a 40 minute interval where ambient temperature drops 2.6 C. A temperature coefficient for the DAC of 44 ppm/°C at a 10 V full scale is estimated from this data.

Stability under local feedback was implemented using the internal ADC to compensate for DAC drift.

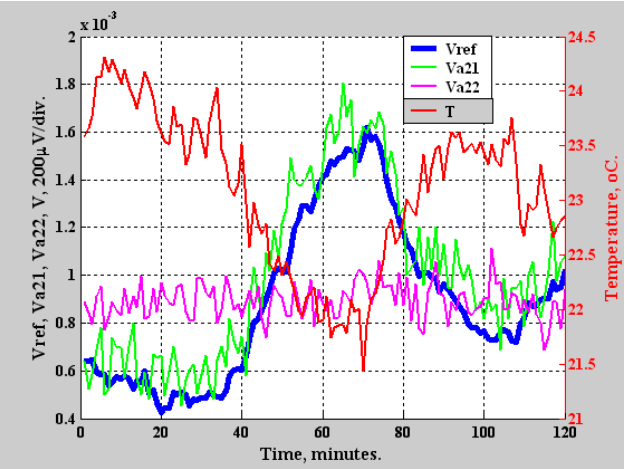

Figure 3. The Vref and Va21 follow the Vsp +10 V DC signal. The Va22 monitors the Vcl.

The test program was run for 50 hours. The average of every 100 points was taken, then averages were analyzed (Fig. 4).

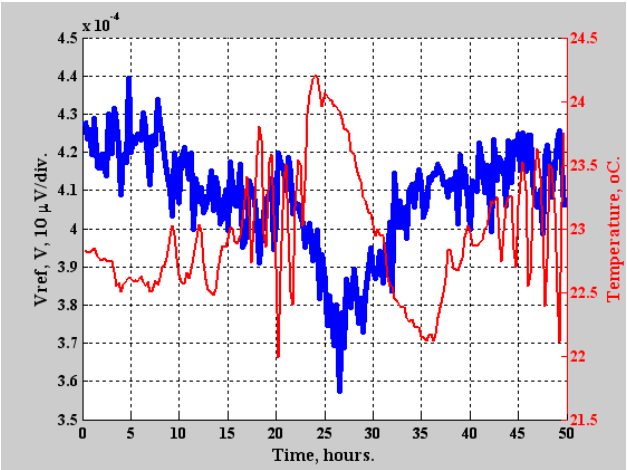

Figure 4. The Vref monitors the DC + 9 V signal of the SP DAC - ADC2 - SP DAC feedback loop.

- The deviation of the averaged data is less than ± 50 μV; not averaged result is ± 200 μV.

At the fast ramp after 23rd hour, Vref drifts to 43 μV (to the minimum), the temperature varies to 1.21 °C.

- Vref ramp drift is 3.6 ppm/°C.

The long slope from 0 to Vref minimum gives the Vref and temperature drifts: 82 μV and 1.7 °C respectively:

- Vref long term slope drift is 4.8 ppm/°C.

Probably, this drift is due to the External Reference 5.4 ppm/°C temperature coefficient at 9 V scale.

The same routine was performed with the CL DAC and ADCs. The Va3 (Vmon) and Va22 (Imon) deviation was ± 300 μV and ± 250 μV respectively. The feedback loop was closed through the ADC2. The feedback signal was bouncing within the CL DAC bit level, after few steps the CL DAC was tuned to the required value and then did not change it over 50 hours. So the feedback was not in use most of the time. The Va3 and Va22 averaged deviations are 74 μV and 54 μV respectively. The maximum temperature drift was about 6 °C, the total drift - 1.2 ppm/°C and 0.9 ppm/°C for the ADC3 and the ADC2 respectively.

SUMMARY

The 170 CANDI corrector power supply controller boards were fabricated and assembled. Their performance was tested and exceeds requirements. Accuracy after the calibration is within ±300 μV at full scale.

Noise on the analog set point voltage varies from 17.7 to 17.3 ENOB. The current read back ranges from 18 to 17.5 ENOB. Stability over 50 hours is about ± 200 μV and 5 ppm/°C for the set point, and ±250 μV and 1 ppm/°C for the analog read back.

The whole system shall be assembled and commissioned on the SPEAR-3 light source.

REFERENCES

[1] G.E. Leyh, et. al. “A Multi-Channel Corrector Magnet Controller,” PAC 95 and IUPAP, Dallas, Texas, 1-5 May 1995

[2] http://www.ti.com/ Burr - Brown Products from Texas Instruments.

[3]http://www.maxim-ic.com/index.cfmMaxim Integrated Products.