A CRITICAL ANALYSIS OF IGBT GEOMETRIES, WITH THE INTENTION OF MITIGATING UNDESIRABLE DESTRUCTION CAUSED BY FAULT SCENARIOS OF AN ADVERSE NATURE

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Abstract

Megawatt class Insulated Gate Bipolar Transistors [IGBTs] find many uses in industrial applications such as traction drives, induction heating and power factor correction. At present, these devices are not optimized for higher speed pulsed-power applications, such as kicker magnets or klystron modulators.

This paper identifies fundamental issues that limit the dI/dt performance of standard commercial packages, and investigates several IGBT design optimizations that significantly improve high-speed performance at high peak power levels.

The paper presents design concepts, results of electromagnetic simulations, and performance data of actual prototypes under high dI/dt conditions.

INTRODUCTION

The prototype 8-Pack modulator for the Next Linear Collider employs an array of commercial 3.3kV IGBT's [Mfr 'A'] for the primary drive stages. Early prototype testing has shown that these IGBTs are susceptible to damage from hard arcs in the 500kV output circuit. A number of failed IGBT's were carefully dissected and analyzed, in order to determine the mechanisms of failure.

Datasheet specifications for the Mfr 'A' IGBT:

V_{CES}	3300V
I_C	800A
I_C [1mS]	1600A
I_{SC} [10uS]	4000A [at 15V V_{GE}]
$V_{CE\,sat}$ [800A]	3.40V

Measurements have shown that peak IGBT currents can exceed 15kA during an arc, with risetimes greater than 10kA/uS. Ideally, the IGBT is supposed to come out of saturation around 4000A (with 15V gate drive) and self-limit its fault current to somewhere around that level.

ANALYSIS OF THE IGBT GEOMETRY

In order to cleanly open the failed units for inspection, an arbor press was used to separate the outer casing from the internal IGBT structure, using a machined support fixture to preserve the internal die substrate and the busbars of the IGBT.

The Mfr 'A' IGBT design employs 16 total IGBT dies and 8 anti-parallel diodes. **Figure 1** shows the placements of the dies. Four separate 'rafts' carry 4 IGBT dies and 2 diode dies each. Positions indicated by 1A - 4D are the IGBT dies, and the 8 blank squares show the anti-parallel diode locations. The emitter and collector busbars connect to the 4 die rafts at points marked by 'E' and 'C'.
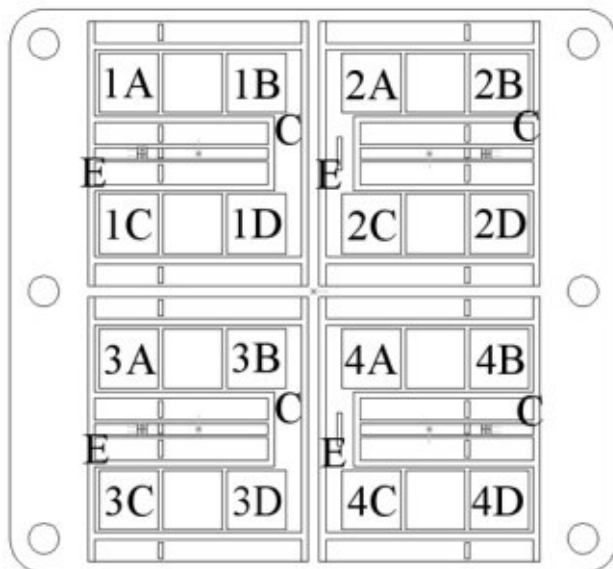

Figure 1: Internal Layout of the Mfr 'A' IGBT.

The points of failure on the actual dies are readily observable. In several cases the entire die is fragmented and blown clear of the pad. The failed die positions are summarized in **Table 1** below, for six failed units:

Table 1: Damage Summary

Die Position	# Of Observed Failures
1C	5
2C	4
3A	2
4C	2

Several patterns are readily apparent in the die failures:

- Dies tend to fail closest to the Emitter terminal.
- Dies tend to fail on the lower half of the raft.
- Dies tend to fail in the upper half of the IGBT.

It is also important to note that on **every** damaged die found, the point of failure was located in the half of the die closest to the emitter busbar.

Each of these four tendencies has the potential for reducing the available silicon by up to 50% during a fault. The aggregate reduction of available silicon from all four effects could therefore be as high as 87.5%. Such an acute constriction of the IGBT's active silicon area would in effect violate the Short Circuit Safe Operating Area by many times during a fault.

EM CURRENT DENSITY SIMULATIONS

Figure 2 shows two EM simulations, with current density profiles for the Mfr 'A' and Mfr 'B' internal IGBT bonding wires and busbars during fast dI/dt conditions. The conductivity of copper is assigned to all conductors. A thin red rectangle around a conductor path indicates where the specified dI/dt is injected. Only half of each complete IGBT module is modeled here, since each module uses two identical sections. The typical matrix computation time for each simulation was approximately 4 hours.

The 8 IGBT dies shown in the Mfr 'A' IGBT have emitter-bonding wires daisy-chained across them, towards the busbars at the center. The hot spots of calculated current density seen on the bonding wires appear to correlate well with the observed damage locations outlined in Table 1 and Figure 1. The simulation also predicts that the portions of the dies closest to the emitter busbars carry the greatest load, by a wide margin.
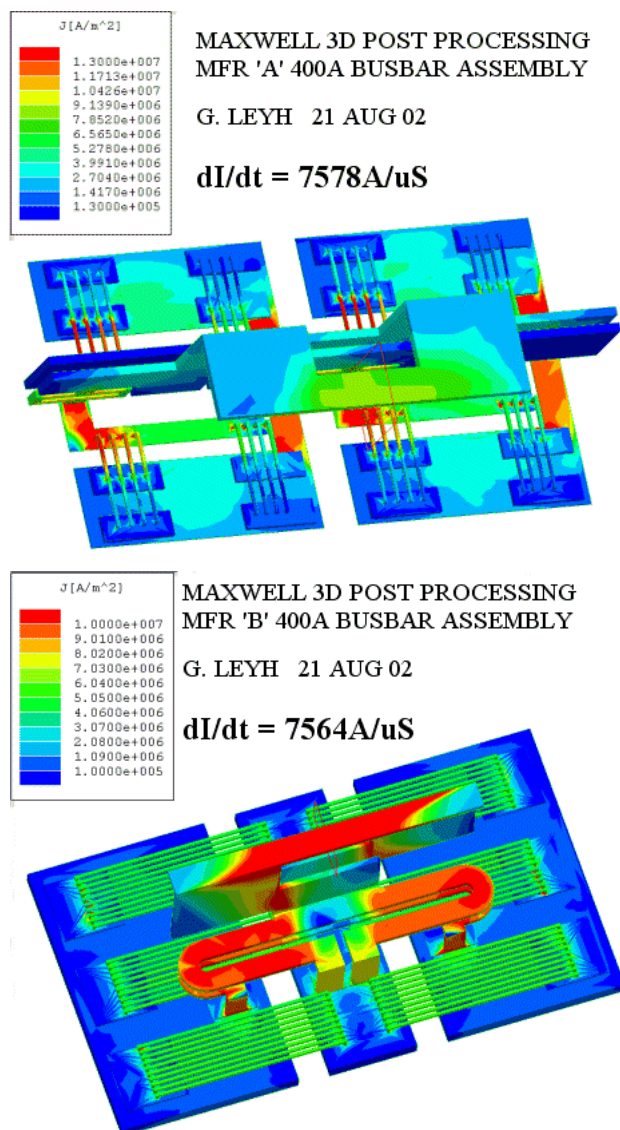
The centralized emitter plate and the long bonding wires of the Mfr 'B' IGBT greatly enhance its current uniformity, as seen in the simulation. Unfortunately this particular IGBT employs a PT silicon technology with a long turn-off tail -- too slow for the NLC application.

A number of design ideas naturally flow from these results. One is a radially symmetric geometry, with a low inductance buswork. **Figure 3** shows the simulated performance of this design. Note that the range of current densities in the bonding wires is less than a factor of two.
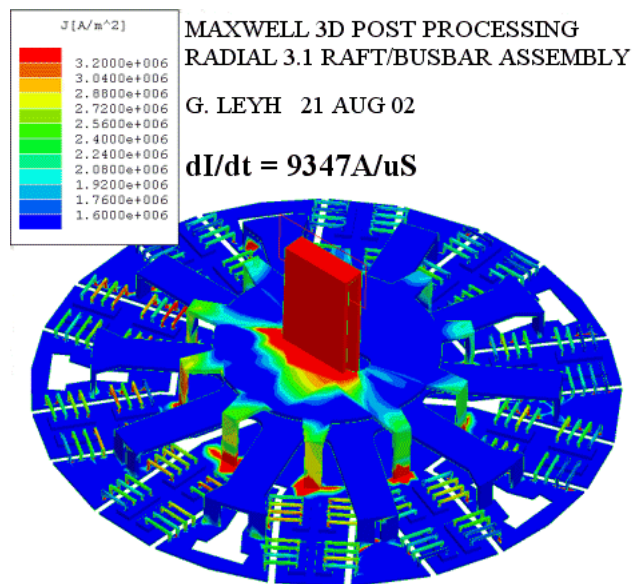

Figure 3: Radial IGBT current density patterns.

Another design concept, though not quite as optimized as the radial approach, is the rectilinear arrangement shown in **Figure 4.** This design has the advantage of improved manufacturability, and compatibility with existing IGBT module footprints. As can be seen, the loss of current sharing performance is minimal. The large blue rectangle in the center is a central emitter summing plate. The green bar represents a parallel plate feed line.
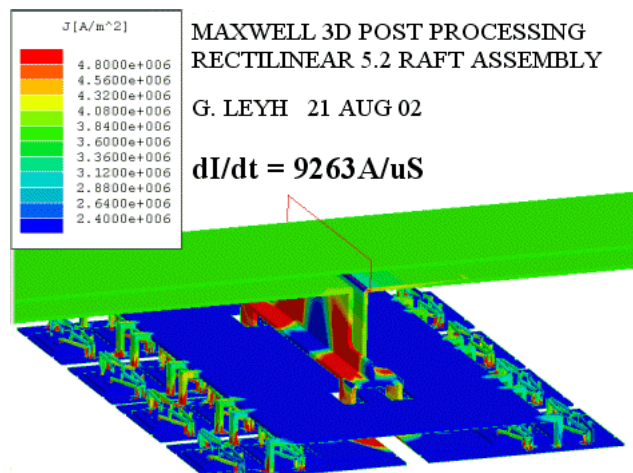

Figure 2: IGBT Mfr 'A' and 'B' current density patterns.

Figure 4: Radial IGBT current density patterns.

PROTOTYPE DESIGN

To evaluate real-world performance parameters, SLAC produced a number of IGBT module prototypes based on the rectilinear concept, using both 3.3kV and 6.5kV IGBT dies provided by Mfr 'A'. The mechanical design of the die substrates, buswork and packaging was performed in-house, based on the simulation results. **Figure 5** shows an exploded isometric view of the prototype IGBT module.
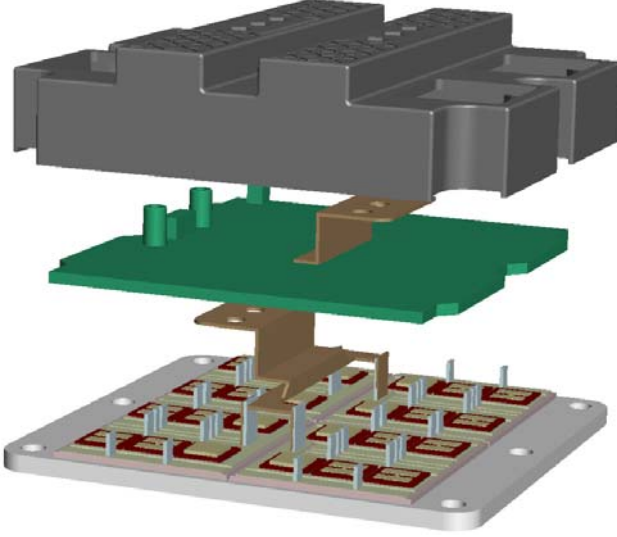

Figure 5: Rectilinear Prototype IGBT assembly.

This design features a number of optimizations for surviving high dI/dt fault events. The emitter bonding wires leave the dies to each side symmetrically and terminate at a single point, minimizing voltage gradients across the die. The large emitter summing plate (green) equalizes the emitter branch inductances. Singular main terminals for the emitter and collector minimize the effects of external circuit current paths on the internal distribution of currents. High-speed active clamp circuitry located at each raft stabilizes the gate voltages against the Miller capacitance during a severe fault.

PROTOTYPE EVALUATION

The test fixture for evaluating IGBT fault performance utilizes a large tape-wound magnetic core with a single turn winding as the test load. A secondary winding attached to a resistive load sets the nominal output pulse current. The core is biased to saturate at some point during the output pulse, thereby producing a near short-circuit condition.

Figure 6 shows the response waveforms for the Mfr 'A' IGBT. The steep rise in current [green] marks the onset of core saturation, about 3uS into the pulse. The IGBT should self-limit to about 2000A at this gate drive level, but internal effects such as the unbalanced emitter bus inductances and the current pinch effects mentioned earlier force the internal gate voltages to vary widely, resulting in a very non-uniform response of each internal die to the fault currents.
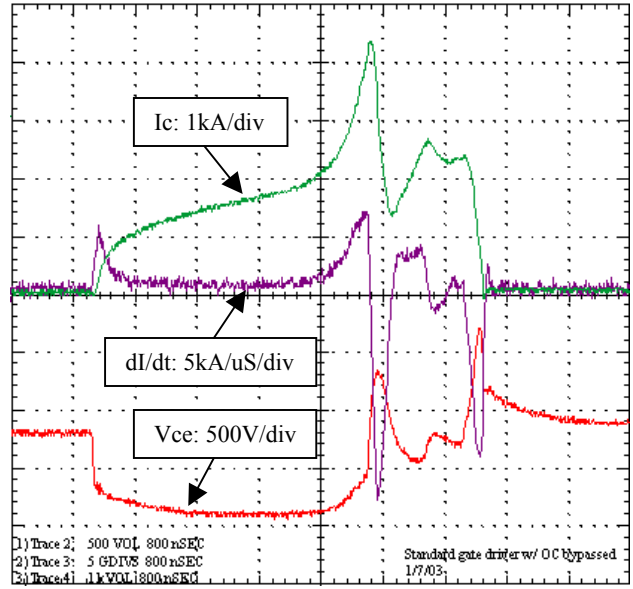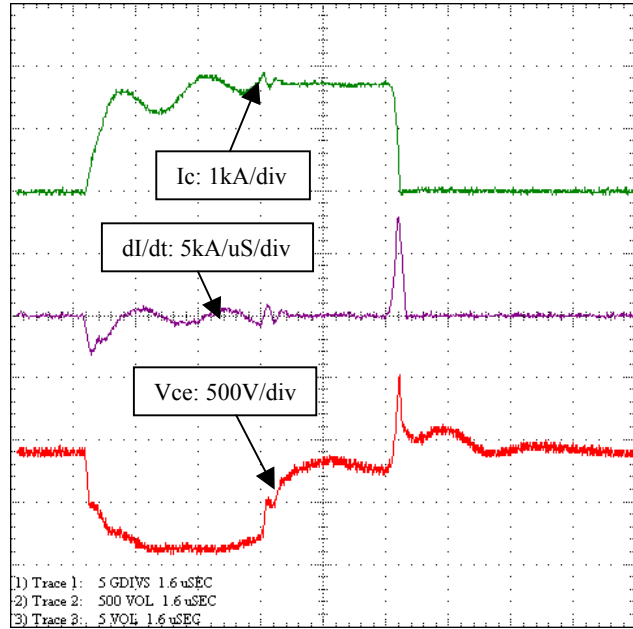

Figure 6: Fault waveforms for the Mfr 'A' IGBT.

Figure 7: Fault waveforms for the SLAC Prototype IGBT.

Figure 7 shows the prototype IGBT operating at roughly the same Vce and output current. The core saturates around 4uS, as can be seen by the rapid rise in Vce [red]. As the impedance of the load approaches a short circuit, the IGBT current flattens around 1800A and Vce approaches the bus voltage. The current overshoot is minimal, owing to the more even current distribution in the emitter buswork and the placement of active gate clamping circuits directly at each of the four internal rafts.

ACKNOWLEDGEMENTS